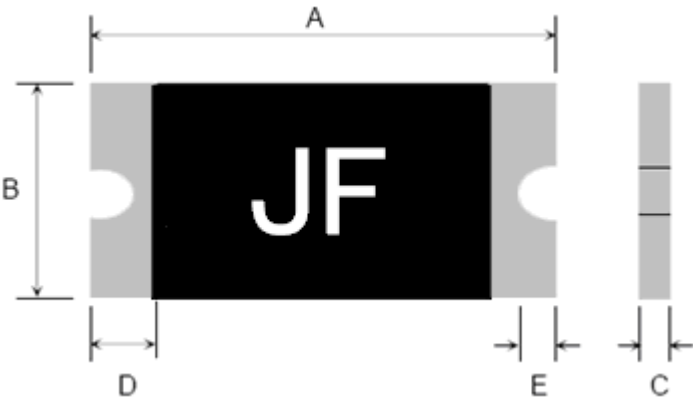


JK-nSMD020 PPTC DEVICES

Part Number: Q/JKTD-24-020

Edition: A0

Page No: 1 OF 3



Terminal pad materials :Tin-Plated Nickle-copper

Terminal pad solderability : Meets EIA specification
RS 186-9E and ANSI/J-STD-002 Category 3.

Marking : JF=1206(020)

Table1 :DIMENTION(Unit : mm)

Model	Marking	A		B		C		D	E
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Min.
JK-nSMD020	JF	3.00	3.50	1.50	1.80	0.40	0.90	0.15	0.10

Table2 :PERFORMANCE RATINGS:

Model	V _{max}	I _{max}	I _{hold} @25℃	I _{trip} @25℃	P _d Typ	Maximum Time To Trip		Resistance		
						Current	Time	R _{i min}	R _{i typ}	R _{l max}
	(Vdc)	(A)	(A)	(A)	(W)	(A)	(Sec)	(Ω)	(Ω)	(Ω)
JK-nSMD020	24.0	100	0.20	0.46	0.6	8.0	0.08	0.35	0.70	3.500

Table3:Test Conditons and Standards

Item	Test Conditon	Standard
Initial Resistance	25℃	0.3500~3.50Ω
I _H	25℃, 0.25A, 60min	No Trip
T _{trip}	25℃, 8.0A	≤0.08s
Trip endurance	24V, 100A, 1hr	No arcing or burning

Operating Temperature: -40℃ TO 85℃

Packaging: Bulk ,5000 pcs per bag

JK-nSMD020 PPTC DEVICES

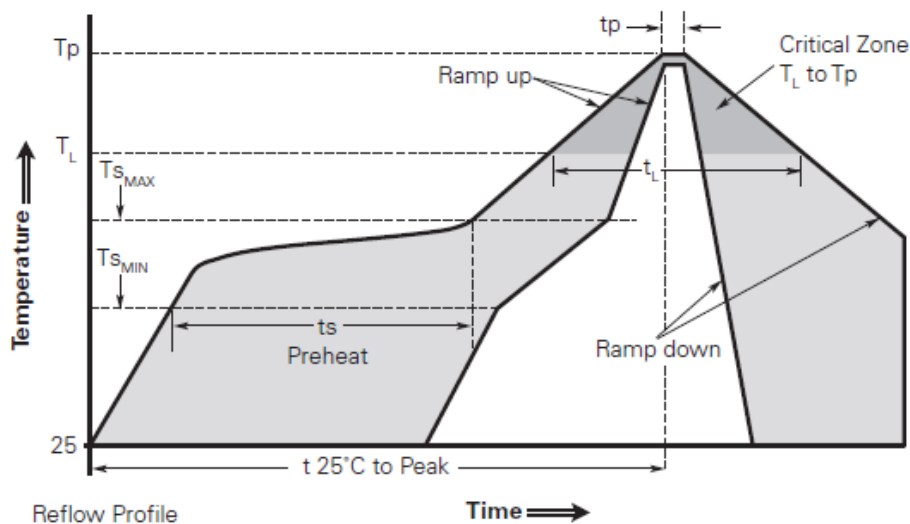
Part Number: Q/JKTD-24-020

Edition: A0

Page No: 2 OF 3



Solder reflow conditions



Profile Feature	Pb-Free Assembly
Average ramp up rate (Ts_MAX to Tp)	3°C/second max.
Preheat	
• Temperature min. (Ts_MIN)	150°C
• Temperature max. (Ts_MAX)	200°C
• Time (ts_MIN to ts_MAX)	60-120 seconds
Time maintained above:	
• Temperature (T_L)	217°C
• Time (t_L)	60-150 seconds
Peak/Classification temperature (Tp)	260°C
Time within 5°C of actual peak temperature	
Time (tp)	30 seconds max.
Ramp down rate	3°C/second max.
Time 25°C to peak temperature	8 minutes max.

Note: All temperatures refer to topside of the package, measured on the package body surface.

- Recommended reflow methods: IR, vapor phase oven, hot air oven, N2 environment for lead-free.
- Devices are not designed to be wave soldered to the bottom side of the board.
- Recommended maximum paste thickness is 0.25mm (0.010inch).
- Devices can be cleaned using standard industry methods and solvents.
- Soldering temprature profile meets RoHs leadfree process.

Notes: If reflow temperatures exceed the recommended profile, devices may not meet the performance requirements

JK-nSMD020 PPTC DEVICES

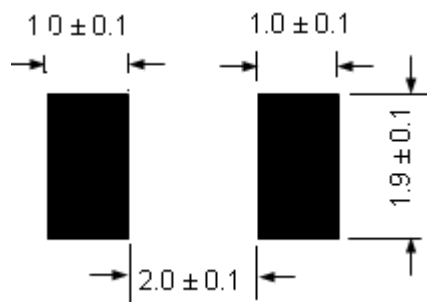
Part Number: Q/JKTD-24-020

Edition: A0

Page No: 3 OF 3



Recommended pad layout (mm)



WARNING

- Use PPTC beyond the maximum ratings or improper use may result in device damage and possible electrical arcing and flame.
- PPTC are intended for protection against occasional over current or over temperature fault conditions and should not be used when repeated fault conditions or prolonged trip events are anticipated.
- Device performance can be impacted negatively if devices are handled in a manner inconsistent with recommended electronic, thermal, and mechanical procedures for electronic components.
- Use PPTC with a large inductance in circuit will generate a circuit voltage ($L di/dt$) above the rated voltage of the PPTC.
- Avoid impact PPTC device its thermal expansion like placed under pressure or installed in limited space.
- Contamination of the PPTC material with certain silicon based oils or some aggressive solvents can adversely impact the performance of the devices. PPTC SMD can be cleaned by standard methods.
- Requests that customers comply with our recommended solder pad layouts and recommended reflow profile. Improper board layouts or reflow profile could negatively impact solderability performance of our devices.